High Speed SPI Bus for Longer Transmission Distances

Abstract

Communications between devices is very common. Many different protocols are already defined in addition to the infinite ways to communicate with a proprietary protocol. Generally, SPI (Serial Peripheral Interface) is used as the inter board communication. This white paper provides an overview of SPI as the external interface using RS422 protocol.

High Speed SPI Bus for Longer Transmission Distances

Overview

Serial Peripheral Interface (SPI) is a widely used serial communication interface in embedded systems. It uses a simple four-wire connection and defined signalling rules. In a typical SPI system, one master device generates the bus clock, and one or more slave devices communicate with it. The four SPI interface lines are:

- **Clock:** Generated by the master to control data transfer.
- **MOSI:** Carries data from the master to the slave.
- **MISO:** Carries data from the slave to the master.
- **Chip Select:** Selects the target slave device and controls access to the interface, especially in systems with multiple slaves.

The figure below shows the interface master and slave device.

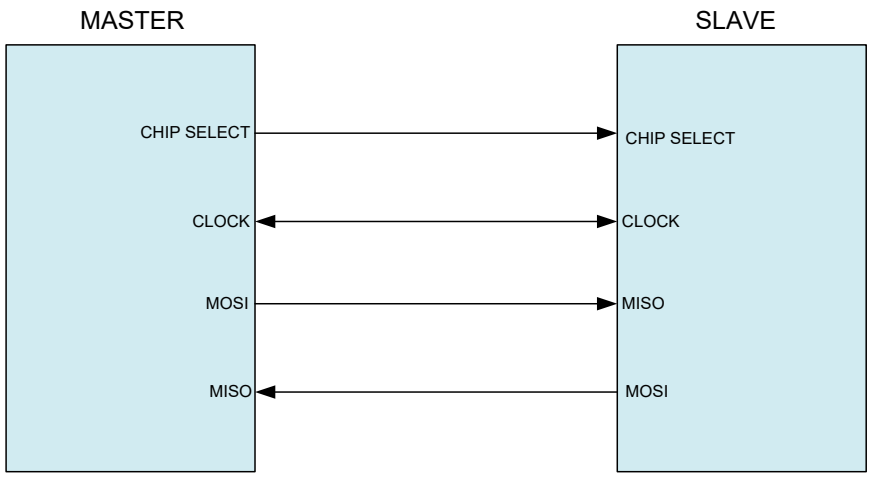

Figure 1: SPI Interface Block Diagram

SPI is commonly used for inter-board communication, but its data rate decreases as the distance between the master and slave devices increases. Over longer distances, propagation delay affects data and clock synchronization, which can lead to data loss or interface failure. In addition, because SPI uses single-ended signalling, it is susceptible to external transients and common-mode noise. These limitations can be addressed by combining a high-speed SPI bus with RS-422 differential signalling.

Discussion

When using the SPI bus as an external interface for long-distance communication, the following issues must be addressed:

- Data-to-clock synchronization errors caused by propagation delay
- Noise interference from unbalanced signal paths and ground-potential differences
- Errors caused by external transients

High Speed SPI Bus for Longer Transmission Distances

In the master-to-slave direction, the transmitted data and the master-generated clock experience the same delay, so they remain synchronized across the link. In the slave-to-master direction, however, the slave begins transmitting only after receiving the first clock edge. The return data then experiences an additional delay before reaching the master, causing it to lag the clock by twice the cable propagation delay. As a result, SPI is not well suited for long-distance signalling and is also vulnerable to external interference that can corrupt data transmission.

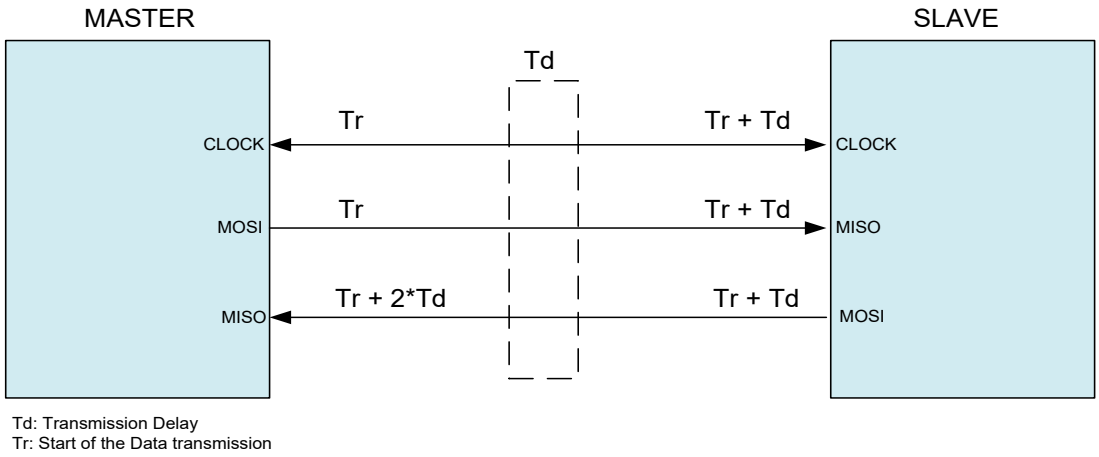

Figure 2: SPI Delay mismatch between Clock to Data

Synchronization error

Synchronization error can be eliminated using two SPI's in the Master as shown in figure 3. In Master, One SPI is configured as the Master and One SPI as Slave. Using this configuration, we can eliminate the synchronization error between Clock and slave data out.

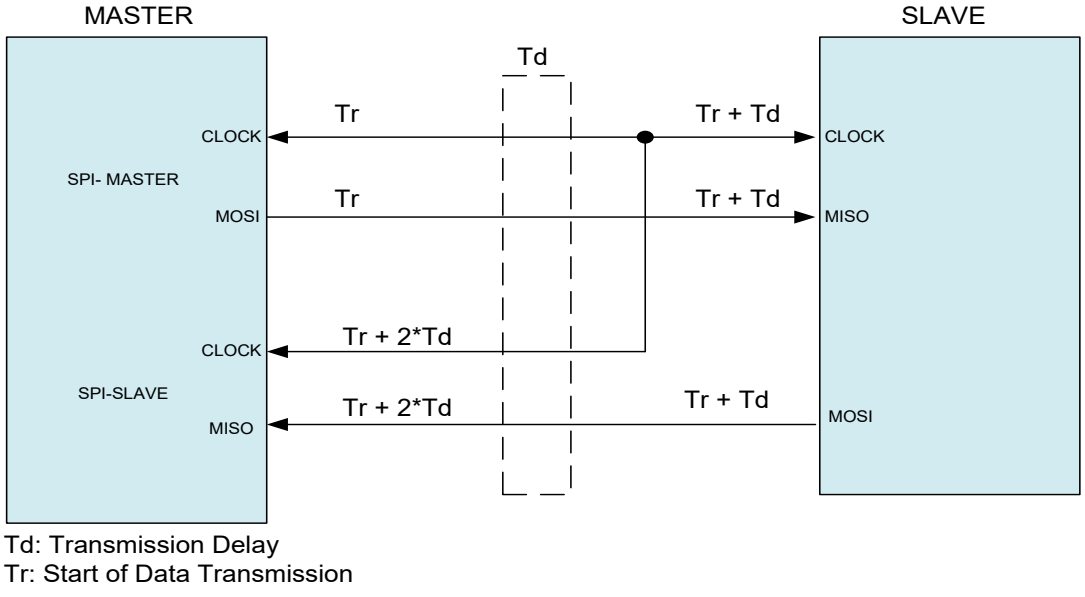

Figure 3: SPI Delay between Clock to Data

High Speed SPI Bus for Longer Transmission Distances

External Noise Interference

Single ended line drive receivers are more prone to the common mode noise and ground imbalance. The Common mode noise can be eliminated using RS422 line driver and line receiver using twisted pair cable. Twisted-pair wire helps prevent radiated EMI (Electro Magnetic Interference), it also helps reduce the effects of received EMI. Because the two wires are close together and twisted, the noise received on one wire will tend to be the same as that received on the second wire.

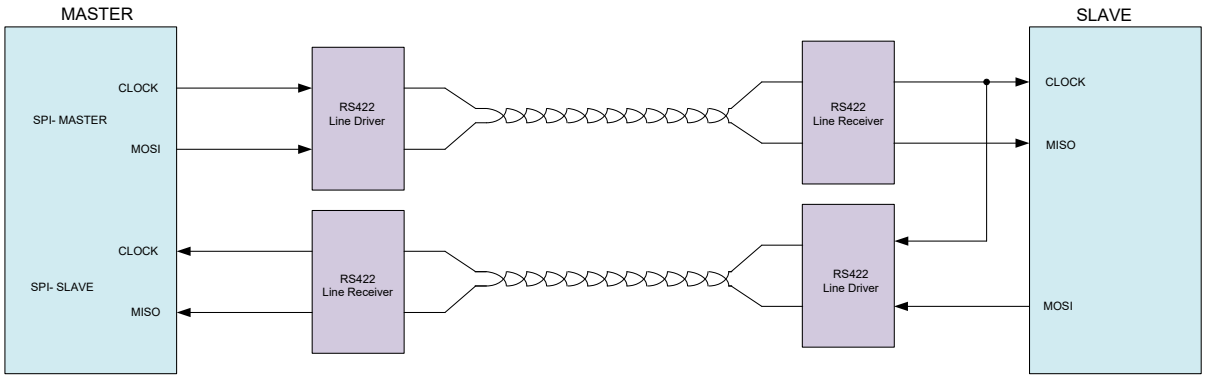

Figure 4: SPI interface with RS422 transceiver

High Speed SPI Bus for Longer Transmission Distances

External Transient

Transient risks. Transients caused by ESD, indirect lightning, or switching of inductive loads can corrupt data transmission and may damage the RS-422 transceivers.

Protection approach. These transceivers can be protected by using suitable transient suppression components, such as TVS diodes and ESD protection diodes.

Low-capacitance implementation. Figure 5 shows a transient protection scheme designed to maintain low capacitance, making it suitable for high-speed transmission.

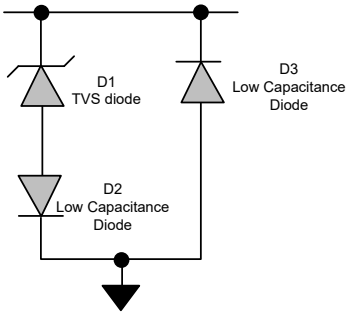

Figure 5: Transient Protection Scheme

The figure below shows the RS-422 transient protection capacitance model,

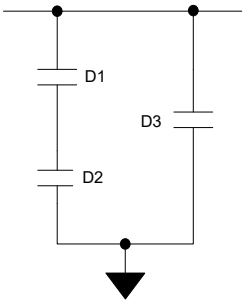

Figure 6: RS-422 Transient Protection Circuit Equivalent Capacitor Model

As shown in the figure 6, TVS diode(D1) will have a parasitic capacitance, which can effectively mitigate the performance degradation in the circuit. Placing a TVS diode in series with a forward biased switching diode (D2, D3) will effectively reduce the total shunt capacitance.

High Speed SPI Bus for Longer Transmission Distances

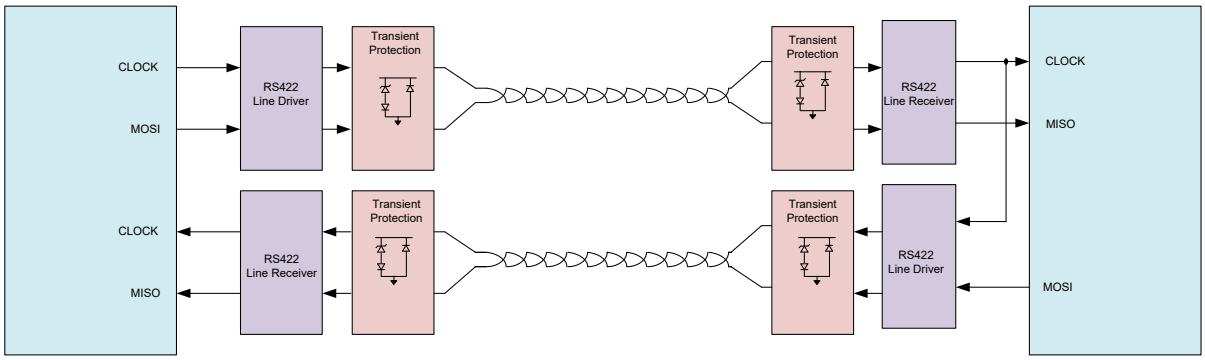

Figure 7: SPI Interface with RS-422 Transceiver with Transient Protection

Conclusion

The SPI bus is used as the intra board communication. SPI can work for longer distance with reduced speed. But SPI with RS422 transceivers, can be used several meters with higher speed.